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CLAIMS

What is claimed is:

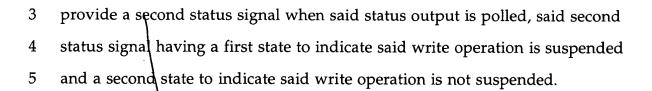
within said control circuit.

1	1. A memory device, comprising:	
2	a memory array;	
3	a register configured to store at least one bit indicating a susp	end status
4	of a write operation; and	
5	a control circuit coupled to said memory array and said regist	er, said
6	control circuit configured to update said register and to control the	output of a
7	status signal representing said suspend status of said write operatio	n.
1	2. The memory device of claim 1, wherein said register r	esides

- The memory device of claim 1, wherein said control circuit is 3. configured to receive a status request signal and said register is configured to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.
- 4. The memory devide of claim 3, further comprising at least one data input/output coupled to said control circuit, wherein at least one data inputs/output is configured to receive said status request signal from a processor and to provide said status signal to said processor.
- 1 5. The memory device of claim 1, further comprising a status 2 output coupled to said register, wherein said status output is configured to

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- 1 6. The memory device of claim 5, wherein said status output 2 represents an output pin.
- 7. The memory device of claim 1, wherein said write operation represents a byte write operation.
- 1 8. The memory device of claim 1, wherein said control circuit
 2 includes a first state machine configured to update at least one of said bits
 3 indicating said suspend status of said write operation in response to a suspend
 4 signal.
 - 9. The memory device of claim 8, wherein said suspend signal represents a byte write suspend command.
- 1 10. The memory device of claim 8, wherein said control circuit
 2 further includes a second state machine coupled to said first state machine
 3 and configured to control the output said status signal in response to a status
 4 request signal.
- 1 11. The memory device of claim 10, wherein said status request 2 signal is a read status register command.

within said control circuit.

1	12. A memory device, comprising:
2	a memory array;
3	a register is configured to store at least one bit indicating a protection
4	status of a data modification operation; and
5	a control circuit coupled to said memory array and said register, said
6	control circuit is configured to update said register and to control the output
7	of a status signal representing said protection status of said data modification
8	operation.
1	13. The memory device of claim 12, wherein said register resides

- 14. The memory device of claim 12, wherein said control circuit is configured to receive a status request signal and said register is configured to output said status signal in response to said status request signal, said status signal having a first state to indicate said data modification operation attempted to access at least one memory location within a protected memory block and a second state to indicate said data modification operation accessed at least one of said memory locations within an unprotected memory block.
- 1 15. The memory device of claim 14, further comprising at least one data input/output coupled to said control circuit, wherein at least one data inputs/output is configured to receive said status request signal from a processor and to provide said status signal to said processor.
- 1 16. The memory device of claim 12, wherein said data modification 2 operation is a programming operation or an erase operation.

		1	17. The memory device of claim 12, wherein said control circuit
•		2	includes a first state machine configured to update at least one of said bits
		3	indicating said protection status of said data modification operation in
		4	response to a block lock configuration signal.
		1	18. The memory device of claim 17, wherein said block lock
		2	configuration signal includes a set block lock bit command.
		1	19. The memory device of claim 18, wherein said control circuit
		2	further includes a second state machine coupled to said first state machine
	O	3	and configured to control the output said status signal in response to a status
	H	4	request signal.
		(K	20. A method of providing the suspend status of a programming
		7/	operation in a memory device, comprising the steps of:
D		3	(a) performing a programming operation to a first memory
	Ú	4	location;
	That	5	(b) prior to the completion of said programming operation,
		6	receiving a suspend signal;
		7	(c) determining whether or not to suspend said programming
		8	operation;
	. **	9	(d) if said programming operation is suspended, updating, if
		10	necessary, a status register to indicate said programming operation is
		11	suspended, and
	\$	12	(e) providing an output signal to indicate said suspend status of
		13	programming operation.

	1	21. The method of claim 20, wherein step (e) comprises the steps of:
	2	(1) receiving a read status register signal; and
	3	(2) providing said output signal in response to said read status
	4	register signal.
	1	22. The method of claim 20, wherein step (e) comprises the step of
	2	providing said output signal at a dedicated status output.
	1	23. The method of claim 20, further comprising the steps of:
	2	(f) performing a second data modification operation to a second
M	3	memory location,
<u> </u>	4	(g) after the completion of said second data modification operation,
<u></u>	5	updating, if necessary, said status register to indicate said write operation is
14 51	6	not suspended; and
	7	(h) resuming said first data modification operation.
COLLOS COLLOS	1	24. The method of claim 23, wherein said second data modification
	2	operation is a read operation.
•	20	25. The method of claim 20, further comprising, prior to step (a), the
Q ¹	2	step of:
and	3	(f) initializing said status register to indicate said write operation is
	4	not suspended.
	1	26. A method of providing the protection status of a data
	2	modification operation in a memory device, comprising the steps of:

3	(a)	performing a data modification operation to a memory location;
4	(b)	determining said protection status of said memory location;
5	(c)	providing an output signal to indicate said protection status of
6	said memory location.	
1	27.	The method of claim 26, wherein step (c) comprises the steps of:
2	(1)	receiving a read status signal; and
3	(2)	providing said output signal in response to said read status
4	signal.	
1	28.	The method of claim 26, further comprising, prior to step (a), the
2	step of:	
3	(d)	initializing a status register to indicate said memory location is
4	protected from data modifications.	
1	29.	The method of claim 26, wherein step (b) comprises the steps of:
1 2	29. (1)	The method of claim 26, wherein step (b) comprises the steps of: performing a read operation to a location within a block lock
	(1)	